REMARKS

The Examiner is thanked for the thorough examination of this application. The Office Action, however, has continued to reject all presented claims 1-30.

Claims 1-2 and 4-30 remain in this application. Claims 1, 6, 23, 24 have been amended. Specifically, claim 1 has been amended to add the limitations of "which extends under and around said first drain diffusion," recited in original claim 6. Claim 6 has been correspondingly amended to delete the limitation of "which extends under and around said first drain diffusion." Claim 23 has been added to incorporate the limitations of "wherein said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region" recited in original claim 24. Claim 24 has been correspondingly amended to deleting the limitation of "wherein said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region."

Double Patenting Rejections

The Office Action has tentatively rejected claim 23 under the judicially created doctrine of obviousness-type double patenting, as being obvious in view of claim 1 of U.S. paten 6,682,993. Applicant has amended independent claim 23 herein, and submits that the amendment to claim 23 addresses and renders moot the double patenting rejection.

The Office Action also rejected claim 24 of the present application as being the same invention of claim 1 of U.S. patent 6,682,993. Claim 24, which depends from claim 23, has also been amended herein. Again, Applicant submits that the amendments made herein to claims 23 and 24 serve to address and overcome the double-patenting rejections.

Claim Objections

Claim 12-22 were objected to "because the claim limitations [Claim 12, lines 10-13, multiple regions of a third dopent type and a special fourth dopent region]" were allegedly not supported by the material in the specification. Applicant respectfully disagrees. In this regard, paragraph [0036] of the present specification states "special diffusion 128 of opposite dopent to the N+ region (122, 124), and therefore of similar dopent to the substrate, but of higher concentration." Accordingly, the specification clearly supports the four different dopent types as claimed, and these claim objections should be withdrawn.

35 U.S.C. 102(b)

Claim 23 was rejected under 35 U.S.C. 102 as allegedly unpatentable over the acknowledged prior art. Claim 23 has been amended herein.

As amended, claim 23 recites:

> 23. A method of forming a protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said method comprising:
>
> connecting source region of a used PMOS device and the source and gate of an unused PMOS device to a first voltage source;
>
> connecting the drains of said used and unused PMOS devices to said active devices input/output pad;
>
> connecting the drain of said used PMOS device to a drain of a first used NMOS device, and the drain of said unused PMOS device to a drain of a first unused NMOS device;
>
> connecting the gate of said used PMOS device and the gate of a second used NMOS device to separate logic signal lines;
>
> connecting the gates of said first used and said first unused NMOS devices to said first voltage source;
>
> connecting the source of said first used NMOS device to the drain of said second used NMOS device and connecting the source of said first unused NMOS device to the drain of a second unused NMOS device;

connecting the source of said second used NMOS and the source and gate of said second unused NMOS device to a second voltage source; and

connecting said ESD protection discharging means for discharging ESD energy appearing between and further directly connected to said first and second voltage source, ***wherein said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region***.

The acknowledged prior art does not teach or suggest the emphasized feature of *said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region.* Instead, the ESD protection discharging means disclosed in the acknowledged prior art is between and further directly connected to said first and second voltage source, but the discharging NMOS device in the ESD protection discharging means of *AAPA does not has a special diffusion region under and around said device normal drain region.*

For at least this reason, claim 23 is allowable. Insofar as claim 23 is allowable, claims 24-30, which depend from claim 23 and its related claims, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 23.

35 U.S.C. 103(a)

Claims 1-2, 4-11 were rejected under 35 U.S.C. 103 (a) as allegedly unpatentable over the acknowledged prior art, in view of Chen et al. (US Patent No. 6,858,900). Applicant respectfully requests reconsideration for at least the reasons set forth below.

Claim 1

As amended, claim 1 recites:

1. A protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said circuit comprising:

at least one switching circuit string composed of a first and second NMOS device and a PMOS device , wherein the gate of said first NMOS device is connected to a first voltage source and the drain element of said first NMOS device is connected to said active devices input/output signal pad and to the drain element of said PMOS device, and the source of said first NMOS device is connected to the drain element of said second NMOS device and the gates of said second NMOS and said PMOS are connected to an internal circuit and the source of said second NMOS is connected to a second voltage source, and the source of said PMOS is connected to a first voltage source; and

a protection discharging means for discharging ESD energy appearing between said first and said second voltage source, wherein said protection discharging means comprising a discharging NMOS device with a first and a second drain diffusion ***which extends under and around said first drain diffusion***, the drain of said discharging NMOS device is directly connected to said first voltage source, and the source of said discharging NMOS device is directly connected to said second voltage source.

(*Emphasis added.*) Neither AAPA nor Chen teach, disclose, or suggest a second drain diffusion which extends *under and around* said first drain diffusion. In this regard, Chen discloses p+ pockets 40 can be selevtively formed *under* any island or any poly gate within the MOS structure not *under and around* said first drain diffusion. For at least this reason, claim 1 defines over the cited art.

Insofar as claim 1 is allowable, claims 2, 4-11, which all depend from claim 1, are also allowable on their own merits in claiming additional elements not included in claim 1.

Claim 12

Claims 12-22 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over the acknowledged prior art, in view of Jung (US Patent No. 5,932,916). Applicant respectfully requests reconsideration of this rejection.

Claim 12 recites:

12. An effective Vcc to Vss power ESD protection device with reduced junction breakdown voltage connected between Vcc and Vss power bus lines comprising:

a substrate having a first dopent type;

isolation regions within said substrate for isolation of said ESD protection device;

a FET gate with abutting spacers for said ESD protection device;

multiple regions of a second dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;

multiple regions of a third dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;

a special fourth dopent region of similar dopent to said substrate beneath one said second and third dopent region;

a protective insulation layer over said ESD protection device; and

first, second and third electrical conductor elements.

(*Emphasis added.*) Neither AAPA nor Jung teach, disclose or suggest a special fourth dopent region of similar dopent to said substrate *beneath one said second and third dopent region*. Instead, Jung discloses *a fourth impurity region 57 formed in a portion of substrate 50, placed on both sides of floating gate electrode 54*, and not *beneath one said second and third dopent region*, as specifically claimed.

For at least this reason, Applicant believes that claim 12 is allowable over the cited reference. Insofar as claim 12 is allowable, claims 12-22, which all depend from claim 12, are also allowable on their own merits in claiming additional elements not included in claim 12.

Conclusion

For the reasons as described above, independent claims 1, 12, and 23 are allowable over the cited references. Insofar as all independent claims are allowable, all claims are allowable.

If the Examiner believes that a teleconference would expedite the prosecution of this application, the Examiner is hereby invited to call the undersigned at the address and telephone listed below.

No fee is believed to be due in connection with this amendment and response. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

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